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1 [Physical Experimentation with Prefetching Helper Threads on Intel's Hyper-Threaded Processors](#)

Dongkeun Kim, Steve Shih-wei Liao, Perry H. Wang, Juan del Cuvillo, Xinmin Tian, Xiang Zou, Hong Wang, Donald Yeung, Milind Girkar, John P. Shen
 March 2004 **Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization CGO '04**

Publisher: IEEE Computer Society

 Full text available: pdf(264.47 KB) Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

Pre-execution techniques have received much attention as an effective way of prefetching cache blocks to tolerate the ever-increasing memory latency. A number of pre-execution techniques based on hardware, compiler, or both have been proposed and studied extensively by researchers. They report promising results on simulators that model a Simultaneous Multithreading (SMT) processor. In this paper, we apply the helper threading idea on a real multithreaded machine, i.e., Intel Pentium 4 processor with Hyp ...

2 [Speculative multithreaded processors](#)



Pedro Marcuello, Antonio González, Jordi Tubella
 July 1998 **Proceedings of the 12th international conference on Supercomputing**

Publisher: ACM Press

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Keywords: control speculation, data dependence speculation, data speculation, dynamically scheduled processors, multithreaded processors

3 [Clustered speculative multithreaded processors](#)



Pedro Marcuello, Antonio González
 May 1999 **Proceedings of the 13th international conference on Supercomputing**

Publisher: ACM Press

 Full text available: pdf(1.17 MB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: clustered processors, control-flow speculation, data dependence speculation, data value speculation, dynamically scheduled processors, simultaneous multithreaded